

# Development Signal Processing Integrated Circuit for Position Sensors with High Resolution

G.V. Prokofiev, K.N. Bolshakov and V.G. Stakhin

**Abstract** The article deals with the problem of creating application-specific integrated circuits transducer signal for position sensors with high resolution. The results of the work on the development of such chips considered various solutions converters angle to code and justify the chosen architecture of the converter on the basis of a digital servo system with interpolation of the input signal. The results of modeling and experimental studies and comparison of developed angle to code converter with other known solutions are described.

**Keywords** Encoder ASIC · Position sensor · Rotary encoder · Resolvers  
Angle sensor

## Introduction

Position sensors are widely used in many industries, in particular, this throttle position sensor and electronic power steering in cars, the sensors of the angular position of the rotor brushless motors, position sensors of mobile elements in robotics, position sensors in machine tools and industrial equipment, etc. Such sensors consist of sensitive element and special electronic processing circuit for calculating position code. Sensitive elements of the sensors are used in different principles, including magnetical elements (Hall-effect or magnetoresistive sensors),

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G.V. Prokofiev (✉) · K.N. Bolshakov · V.G. Stakhin  
VLSI Department, Zelenograd Nanotechnology Center, Moscow, Russia  
e-mail: prokofiev@idm-plus.ru

K.N. Bolshakov  
e-mail: bolshakov@idm-plus.ru

V.G. Stakhin  
e-mail: stakhin@zntc.ru

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sine-cosine encoders, sine-cosine resolvers, linear differential transformers (LVDT), or optical sensor systems.

The main trend is the integration of all processing circuitry into a single chip for the purpose of miniaturization of sensors, reducing their costs, and increasing the reliability [1]. Another major trend in the development of signal processing schemes is to increase the resolution of the conversion. For many of actual tasks necessary to provide an angular resolution of one period of sine-cosine signal 15–16 bits and higher.

Also to ensure the greatest breadth of applications, it is necessary to carry out the processing of the signals from all of the most common sine-cosine sensor systems, including resolver, LVDT, sine-cosine magnetic, and optical systems.

## Objective

The aim is to develop a single-chip application-specific integrated circuit (ASIC), which provides processing of signals from the position sensors of all major types, with a resolution up to 16 bits per one period of the input sine-cosine signal.

## Development of Signal Processing Integrated Circuit

To achieve the stated purpose is required to integrate the single-chip system for generating a drive signal for resolver, LVDT, and specialized signal demodulator with the secondary windings of the transformer, converter angle code, LVDT signal processing unit, and a channel for generating a reference pulse for optical encoders. A key element of such systems is the angle converter code.

Angle to code converters built on two basic principles—tracking loop converter that minimizes the error signal between the input signal and its image in the transmitter memory (table of sine and cosine) [2], and on the basis of direct calculation of the arc tangent of the angle, the most common of which is a system based on CORDIC algorithms [2, 3].

Angle to code converter with direct calculation has fixed the conversion delay is independent of the input signal phase. However, this architecture is sensitive to the quality of the input signal and does not guarantee monotonicity conversion that is necessary for most control systems where position sensors are used for the feedback. To improve the quality of the input signal in direct conversion systems, the provisional carry signal filtering and processing intensive use different algorithms such as Wavelet transformation [4].

Tracking architecture provides guaranteed monotonic conversion, as it represents the code position counter output count pulses from the generator, and the

frequency of which depends on the polarity of the error signal between the input signal and the sine and cosine images placed in the converter memory [5]. A tracking system in the tracking mode provides maximum performance, but the time of entering the tracking depends on the current phase of the input signal, and in the worst case, equal to the time needed to iterate over all counter values. For most applications, this feature of the tracking system is not critical.

Tracking converter may be implemented as an analog-to-digital system, and completely in the digital domain. The analog-to-digital implementation of the error signal generated in analog form on the multiplied digital–analog converters (DACs). The maximum resolution of this architecture is around 13 bits, which is primarily due to the limited accuracy of the multiplied DACs because of the mismatch of their elements, as well as with the size of such a high-resolution DACs. As an example, commercial chips based on analog-to-digital tracking system can cause chip iC-NQC [6], as well as a single-chip encoder with a resolution up to 13 bits [7]. Can be realized high-resolution analog-to-digital servo converters based on delta-sigma DAC, but this solution will provide low speed.

For conversion accuracy of 14 bits or more is already applied transformation angle code entirely in the digital domain [8]. This makes it easier to make a preliminary mathematical processing of the input signals to compensate for many of non-idealities of the sensor system.

An analysis of architectural solutions in order to achieve high resolution and the lack of a guaranteed pass code has been selected on the basis of the architecture of the full digital tracking converter.

A key element in determining the accuracy of digital processing is an analog–digital converter (ADC). The highest resolution of the ADC has performed on sigma-delta architecture [9]. For converter, a multi-bit sigma-delta modulator of the second order has been developed, made by CIFF architecture (cascade of integrators with feed forward summation) [10]. The modulator converts the input analog signal into a 4-bit sample stream at a frequency of 8 MHz.

Structure of development integrated circuit is shown in Fig. 1.

ASIC consists of internal frequency synthesizer based on direct digital synthesis, it generates sinusoidal signal with programmable frequency and signals amplitude. Sinusoidal signal from synthesizer is used to drive the primary winding of the resolver or LVDT using a delta-sigma DAC.

Detailed conversion signal path for development ASIC is shown in Fig. 2.

ASIC has two conversion channel, includes programmable differential amplifiers PGA1, PGA2 and sigma-delta modulators SDM1, SDM2. The output signal from modulators is fed processing unit provides quadrature demodulation, decimation, and interpolation of the input signal with a resolution of 16 bits and a conversion time of 500 ns. The filter-decimator provides a programmable decimation from 32 to 4096 samples. For the minimum values of decimation, the signal bandwidth is 62.5 kHz. A feature of implemented digital processing system is the interpolation algorithm of the output of ADC samples, allowing to provide a constant value in the

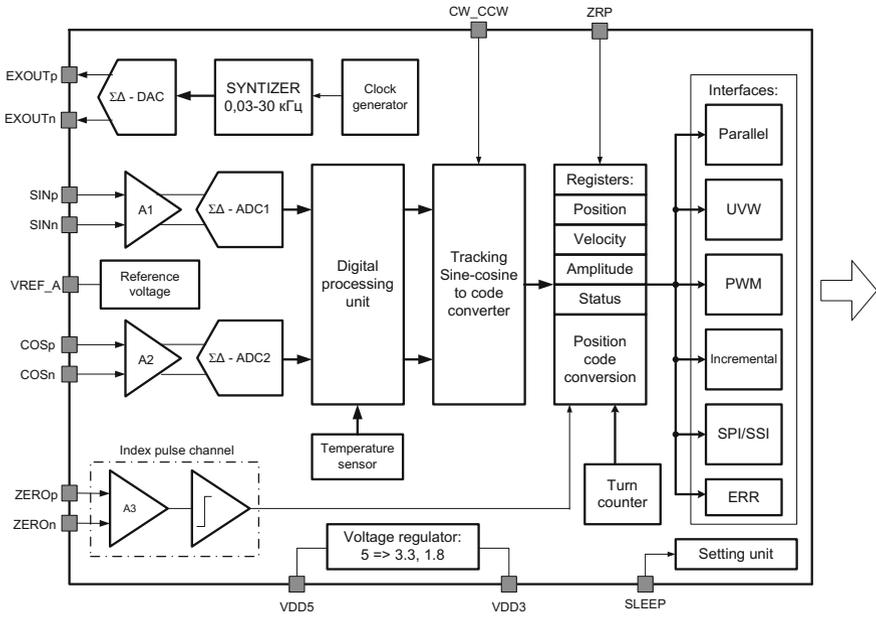


Fig. 1 Structure of development integrated circuit

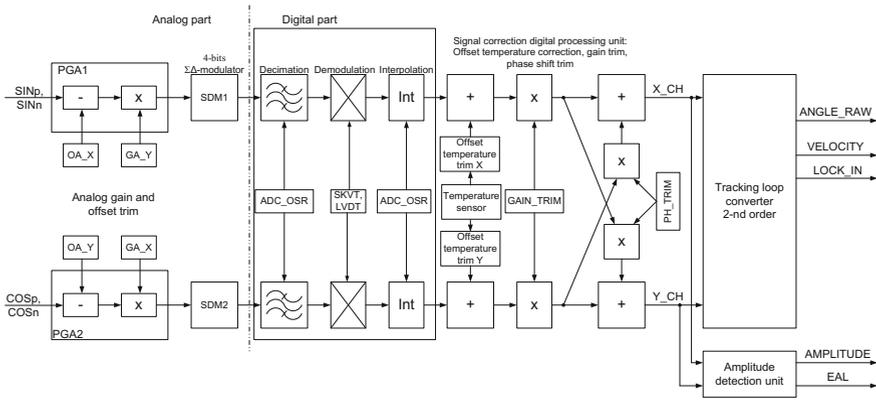


Fig. 2 Conversion signal path of development ASIC

sampling frequency of 2 MHz with 18-bit resolution conversion despite using high decimation of signal values (32–4096). Interpolation is done by filling the intermediate values between the ADC samples with zero values and subsequent processing of the received signal using low pass filter.

Due to the input signal has harmonic type, using interpolation is applicable to the system. This allows the use of ADC with less speed and power consumption, at the same time providing a comparable conversion with converters with significantly more high-speed ADCs.

The filtered and demodulated signal is supplied to the signal correction circuit providing compensation for thermal drift of the offset voltage of input signals by the integrated temperature sensor, independently for each channel, channel gain adjustment, compensation for phase shift between channels.

The corrected signal is supplied to the tracking converter, which converts an input signal into position code with a resolution of 13–16 bits. Next, the code position is adjusted depending on the user settings, counts the number of revolutions, and the combined location code is supplied to the interface circuit.

Structure of tracking loop converter is shown in Fig. 3. Tracking loop converter is minimized error signal *Err* with expression:

$$Err = \sin(\phi) \cdot \cos(Addr) - \cos(\phi) \cdot \sin(Addr)$$

where  $\phi$ —phase of input signal, *Addr*—position counter code.

Error code integrated at Proportional-Integral controller Pi-reg and connects to code control oscillator CCO (analogous to voltage-control oscillator in analog domain). The CCO depends on the magnitude and polarity of the signal from PI-controller that generates counting pulses UP and DN for the reversive counter. Convert counter code into sine and cosine representations used generator based on CORDIC algorithm in rotation mode with pipelined architecture. Traditionally, such systems for storing sine and cosine values corresponding to counter code using

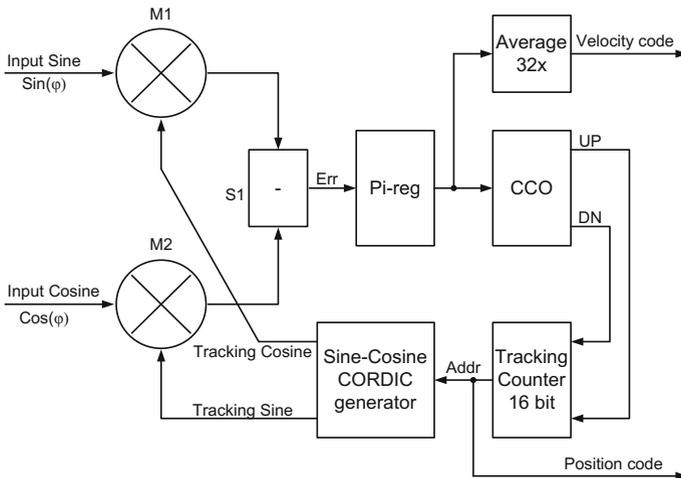


Fig. 3 Structure of designed tracking loop converter

**Table 1** Comparison traditional and proposed converted architectures

Parameter	Resolution 16 bit, 0.6 $\mu\text{m}$ technology		Resolution 12 bit, 0.18 $\mu\text{m}$ technology	
	Traditional solution	Proposed solution	Traditional solution	Proposed solution
	ROM	524.288K	16 bit CORDIC	ROM 24.576K
Occupied area, $\text{mm}^2$	8.2	1.5	0.09	0.035

a non-volatile memory (ROM), usually keep a quarter of the period, and a signal linking to the full period [5]. This solution provides high-speed conversion, but requires large area on die of ASIC. The proposed solution provides a smaller area occupied by the converter, since it requires to store coefficients slight memory of the 14 values of the binary-weighted arc tangent of the angle. Comparison of occupied area was carried for the traditional architecture using a ROM and proposed solutions. The evaluation was conducted for the same technology, for proposed solution using results from digital synthesis on target standard cell logic library. Comparison result shows in Table 1.

The Table 1 shows that the designed solution can significantly reduce the area of tracking converter.

Velocity calculation used averaged signal from PI-controller.

Amplitude calculation used amplitude detector based on iteration CORDIC converter in vector mode.

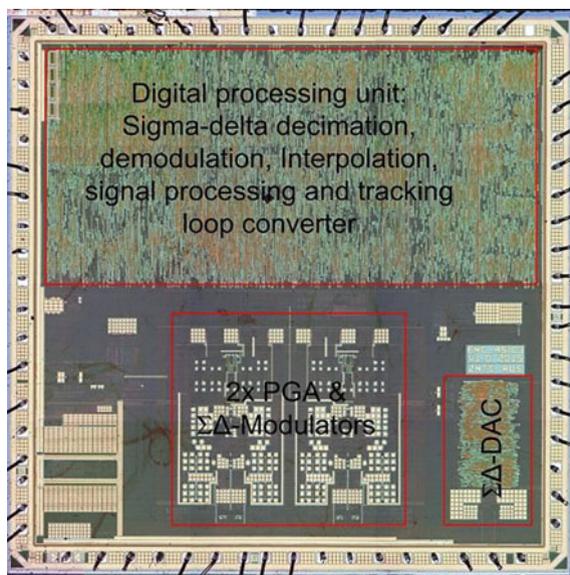
## Examination of Development Integrated Circuit

Development ASIC was fabricated with 180 nm CMOS technology (X-FAB XH018 CMOS process). Die size  $3.6 \times 3.6$  mm. Nominal clock frequency is 16 MHz. Photo of die of fabricated ASIC is shown in Fig. 4.

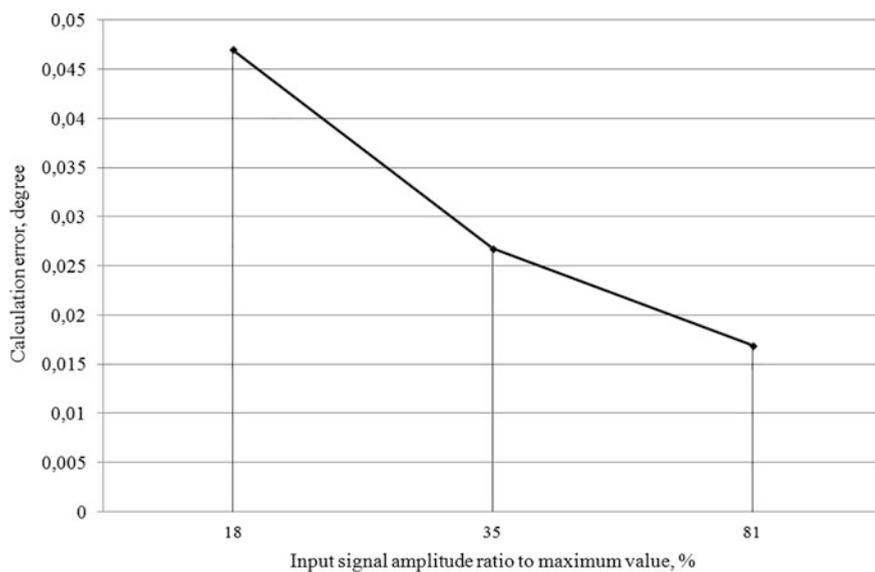
For developed ASIC conversion error of sine-cosine signal in the code was calculated. Testing circuit to determine conversion error is shown in Fig. 4. The input circuit model was applied sine-cosine signal frequency of 15 Hz and different amplitudes. Compared to the position code on the output circuit with a reference angle calculated from the input signal is determined by the conversion error.

Figure 5 shows the values of conversion error from the input signal amplitude (in % of the maximum possible signal amplitude) for the ADC 32 decimation mode (providing the maximum bandwidth of 62.5 kHz bandwidth ADC).

It was studied the effect of the filter characteristics of the digital signal processing unit (decimation factor and interpolation) on the accuracy of the development converter. Results are shown in Table 2.



**Fig. 4** Photo of die of development ASIC



**Fig. 5** Conversion error versus amplitude of input signals

**Table 2** Effect of filter characteristics of conversion error

Decimation	Interpolation	ADC sampling frequency, at system clock 16 MHz, kHz	Total conversion error, degree
32	none	250	0.0169
64	none	125	0.0209
128	32	2000	0.0167
256	64	2000	0.0170
1024	256	2000	0.0174
2048	512	2000	0.0173
4096	1024	2000	0.0174

**Table 3** Conversion error measurement results

Decimation	Interpolation	Conversion error (stationary position), degree	
		Sine-cosine mode	Resolver mode modulation frequency 4.073 kHz
32	0	0.038	–
64	0	0.027	–
128	32	0.022	–
256	64	0.016	–
512	128	0.016	0.016
1024	256	0.011	–
2048	512	0.005	–
4096	1024	0.005	–

Simulation results show that the use of interpolation ADC samples to increase the sampling frequency has virtually no effect on the conversion tracking error transducer. This makes it possible to obtain high-performance converter code angle ADC sigma-delta type for large decimation signal. So for decimation in 4096 samples and at clock frequency of the modulator in 8 MHz we obtain nominal sampling frequency of 1953 Hz, but through the use of interpolation in 1024 points at the filter output we obtain sampling frequency 2 MHz. As shown by the simulation results, the conversion error will not be degraded compared with decimation 32 without using interpolation.

Measurements were conducted with connecting external precision sine-cosine source and with resolver LIR-158. Signal amplitude in both cases was within 90% from maximum value. Measurement results for conversion error are shown in Table 3.

Comparison of development ASIC with others known sine-cosine to position code converter chips is shown in Table 4.

Influence of measuring the ambient temperature has been produced by the conversion error. The measurements were made using an external source of precision sine-cosine signal board with a chip placed in a heat chamber. Measurements were made in the temperature range of  $-60 \dots + 150$  °C. Conversion error over the entire temperature range of samples was 5 or 0.027 degrees.

**Table 4** Comparison of development ASIC with others sine-cosine to position code converter chips

Parameter	Development ASIC	AD2S1210, Analog Devices	iC-TW8, iC-Haus	2602PV2AP, NIIEMP	RD-19230, Data Device Corp.
Angle to code converter architecture	Tracking full digital, 2nd order	Tracking full digital, 2nd order	Direct conversion, CORDIC	Tracking, analog–digital, 2nd order	Tracking, analog–digital, 2nd order
Maximum resolution, bit	16	16	16	16	16
Tracking frequency at maximum resolution, Hz	30	125	n/a	2	18
Settling time at angle step $179^\circ$ for maximum resolution, ms	16	45	n/a	40	50
Conversion error, degree	0.027	0.17	0.08	0.022	0.022
Maximum resolution, bit	48	49	35	270	50
Operating temperature range, °C	-60... + 150	-40... + 125	-40... + 125	-60... + 85	-40... + 85

## Conclusions

The research results show the correctness of the chosen chip architecture. According to the measurement results, achieved conversion accuracy is less than 0.03 angular degrees in temperature range  $-60... + 150^\circ\text{C}$  at a current consumption of 48 mA and a conversion time of 500 ns. Using the algorithm of interpolation ADC samples allowed for a constant conversion rate does not depend on the value of decimation, without significant degradation of conversion accuracy. Research has shown that the use of interpolation ADC samples in order to increase the sample rate does not affect the conversion error of sine-cosine tracking converter. This makes it possible for the same ADC conversion rate to get a much higher sampling frequency, and thus provide more speed of angle to code converter.

Developed ASIC will create angular and linear position sensors with high resolution. Due to the high degree of integration chip capable of processing the signal from the sensors of different types, which makes it fairly wide range of applications.

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